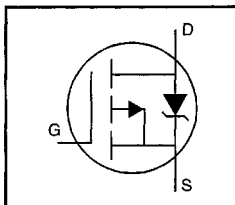


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = -200V$$

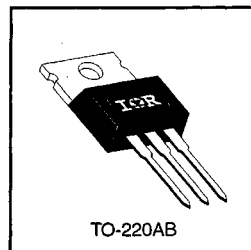
$$R_{DS(on)} = 1.5\Omega$$

$$I_D = -3.5A$$

Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.


 DATA
SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-3.5	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-2.0	
I_{DM}	Pulsed Drain Current ①	-14	
P_D @ $T_C = 25^\circ C$	Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{LM}	Inductive Current, Clamp	-14	A
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} =0V, I _D =-250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.22	—	V/°C	Reference to 25°C, I _D =-1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V _{GS} =-10V, I _D =-1.5A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
g _{fs}	Forward Transconductance	1.0	—	—	S	V _{DS} =-50V, I _D =-1.5A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} =-200V, V _{GS} =0V
		—	—	-500		V _{DS} =-160V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} =-20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} =20V
Q _g	Total Gate Charge	—	—	22	nC	I _D =-4.0A
Q _{gs}	Gate-to-Source Charge	—	—	12		V _{DS} =-160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	10		V _{GS} =-10V See Fig. 11 & 18 ④
t _{d(on)}	Turn-On Delay Time	—	15	—	ns	V _{DD} =-100V
t _r	Rise Time	—	25	—		I _D =-1.5A
t _{d(off)}	Turn-Off Delay Time	—	20	—		R _G =50Ω
t _f	Fall Time	—	15	—		R _D =67Ω See Figure 17 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	350	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	100	—		V _{DS} =-25V
C _{rss}	Reverse Transfer Capacitance	—	30	—		f=1.0MHz See Figure 10



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-3.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-14		
V _{SD}	Diode Forward Voltage	—	—	-7.0	V	T _J =25°C, I _S =-3.5A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	300	450	ns	T _J =25°C, I _F =-3.5A
Q _{rr}	Reverse Recovery Charge	—	1.9	2.9	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

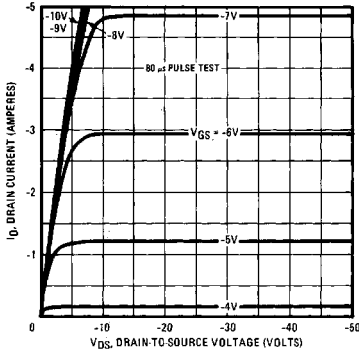
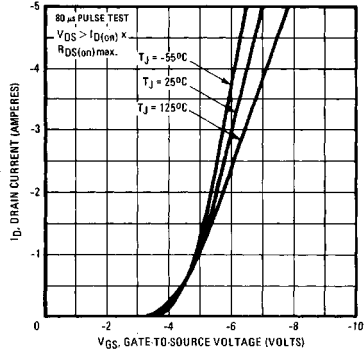
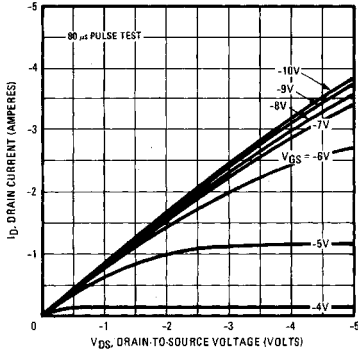
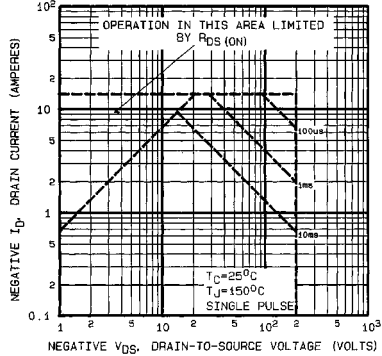
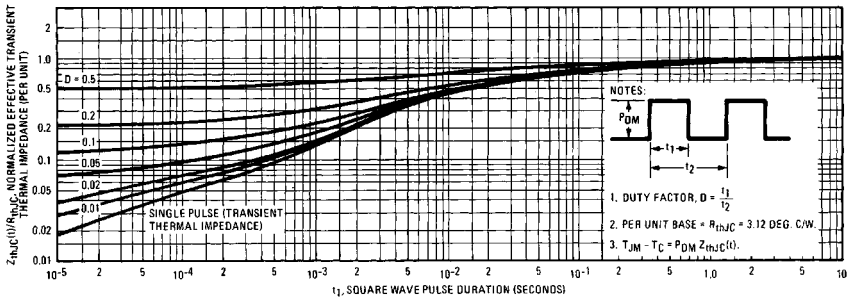
Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 5)

③ I_{SD} ≤ 3.5A, di/dt ≤ 95A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C

② Not Applicable

④ Pulse width ≤ 300 μs; duty cycle ≤ 2%.


Fig. 1 — Typical Output Characteristics

Fig. 2 — Typical Transfer Characteristics

Fig. 3 — Typical Saturation Characteristics

Fig. 4 — Maximum Safe Operating Area

Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

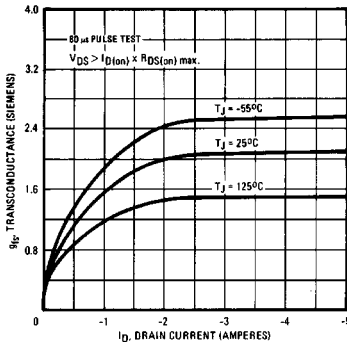


Fig. 6 — Typical Transconductance Vs. Drain Current

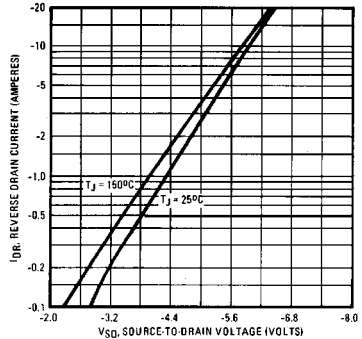


Fig. 7 — Typical Source-Drain Diode Forward Voltage

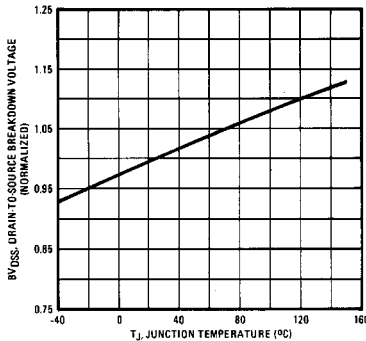


Fig. 8 — Breakdown Voltage Vs. Temperature

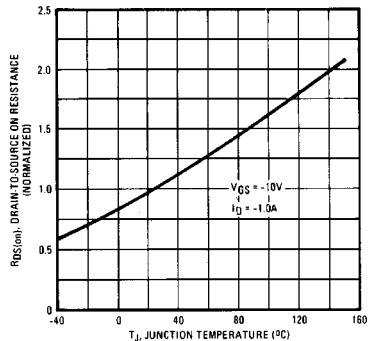


Fig. 9 — Normalized On-Resistance Vs. Temperature

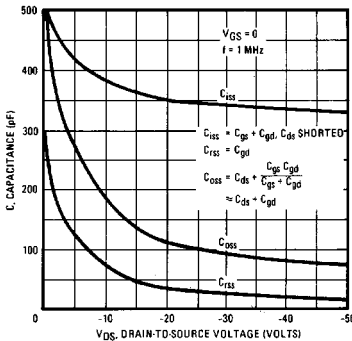


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

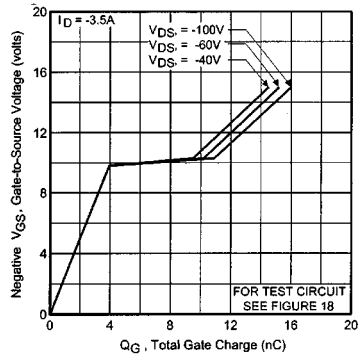


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

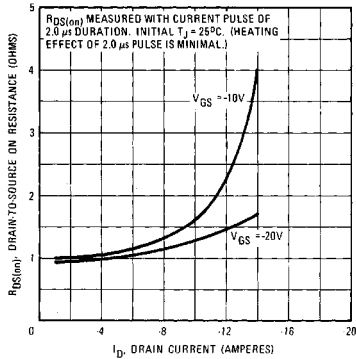


Fig. 12 — Typical On-Resistance Vs. Drain Current

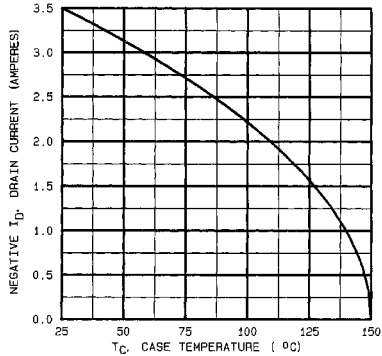


Fig. 13 — Maximum Drain Current Vs. Case Temperature

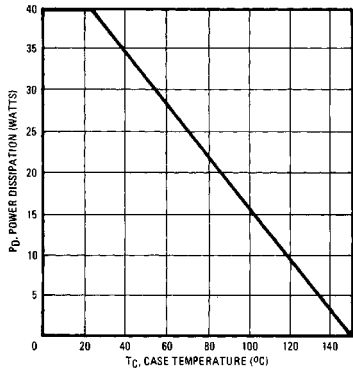


Fig. 14 — Power Vs. Temperature Derating Curve

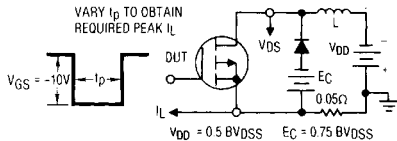


Fig. 15 — Clamped Inductive Test Circuit

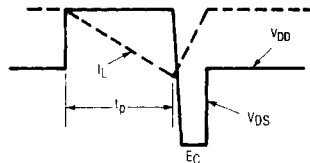


Fig. 16 — Clamped Inductive Waveforms

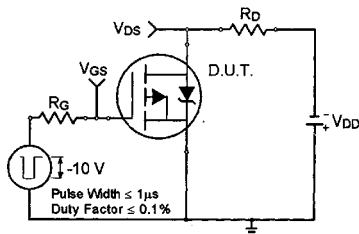


Fig. 17a — Switching Time Test Circuit

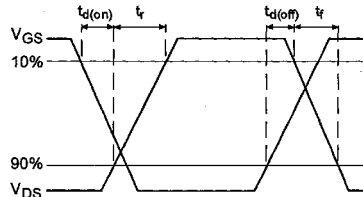


Fig. 17b — Switching Time Waveforms

DATA SHEETS

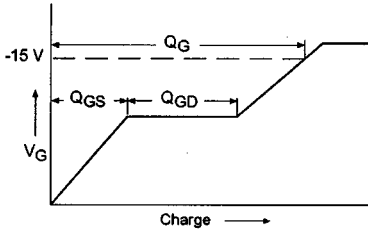


Fig. 18a — Basic Gate Charge Waveform

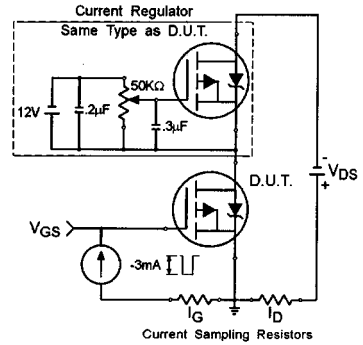


Fig. 18b — Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525